Improvement of a high current DC power supply system for testing the large scaled superconducting cables and magnets

Improvement of A High Current DC Power Supply System for Testing the Large Scaled Superconducting Cables and Magnets

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Abstract----A dc 75 kA power supply system was constructed to test the SC (superconducting) R&D (research and development) cables and magnets for the Large Helical Device (LHD). It consists of three 25 kA unit banks. A unit bank has two double-star-rectifier connections with the inter-phase reactors. A digital feedback control method is applied to the automatic current regulation (ACR) in each unit bank. For shortening the dead time of the feedback process, a new algorithm of a digital phase controller for the ACR is investigated. A Bode diagram of the feedback process is directly measured. It is confirmed that the dead time of the feedback process is reduced to one sixth, and that the feedback gain of PID (proportional, integral and differential) compensation is improved by a factor of two from the original method.

I. INTRODUCTION

The LHD is a fusion experimental device of heliotron type. It consists of fully SC coils with the total stored magnetic energy of 1.6 GJ [1], [2]. It is not easy to fabricate such large coils, so a R&D program to develop the SC cables and its winding technology for the LHD started in 1989 [3], [4]. The SC magnet testing facilities including a cryogenic system of 200 l/h of liquid helium, a 10 MN mechanical testing machine, a test facility of SC short samples and SC R&D magnets have been constructed since 1990. A dc 75 kA power supply system was also equipped, for testing the SC R&D cables and magnets [5].

For a SC short sample, the load impedance is nearly equal to that of a short circuit. The power supply system, therefore, must be a low-impedance system. The double-star-rectifier connection with the inter-phase reactors should be suitable for a low voltage and high current system, because a pair of thyristors is fired at the same time and the thyristors are not connected in series, like a Graetz bridge.

This power supply is composed of three 25 kA unit banks, and each bank has two double-star rectifiers to decrease the ripple of the output voltage. To improve the signal to noise ratio, digital feedback control method is applied to the automatic current regulation in each bank.

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Four SC magnets with the inductance of 3.18 ~ 54 mH and eleven SC short samples have been already tested by using this power supply system [6]-[9]. A time delay of the current rise was observed in the fast ramp operations of large magnets. This delayed response is caused by the large dead time of the feedback process and insufficient feedback gain. We developed a new algorithm of the digital feedback control system for shortening the dead time of feedback process. The control characteristic of the new digital phase controller is also investigated.

II. COMPOSITION OF A DC 75 KA POWER SUPPLY

Fig. 1 gives a circuit diagram of a dc 75 kA power supply system which consists of three 25 kA unit banks (A-1, A-2 and A-3). One unit bank has two double-star transformers with the inter-phase reactors, dc ripple filters and 12-phase rectifiers. A-1 and A-2 units are used for exciting the SC R&D magnets with the inductance of 3.18 ~ 54 mH. They have dc circuit breakers (CB) and commutating resistors (Rc) with diodes for the coil protection. For decreasing the current ripple to the level which is equivalent to that of 24-phase rectification system, the electrical angles of the transformers in A-1 and A-2 are determined to be +7.5° and -7.5°, respectively. In the short sample tests of the SC cables, all of

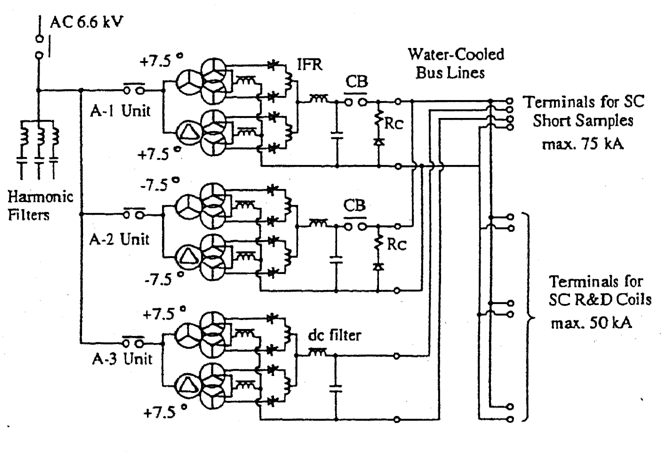

Fig. 1. Circuit diagram of a dc 75 kA power supply.

Table 1. Specifications of the 25 kA unit bank.

AC input voltage	6.6 kV, 3-phase, 60Hz
DC output voltage	8 V or 21 V
DC output current	25 kA
Maximum current ripple	$\leq 10^{-4}$ (for inductive loads) $\leq 10^{-2}$ (for short circuits)
Maximum ramp rate	999 A/s
Rectification	two double star (12-phase)
Current Regulation	digital feedback control (PID compensation)
DC circuit breaker	$\leq$25 kA ($\leq$1 kV)
Commutating resistor	40 mΩ / 5 mΩ (40 MJ)

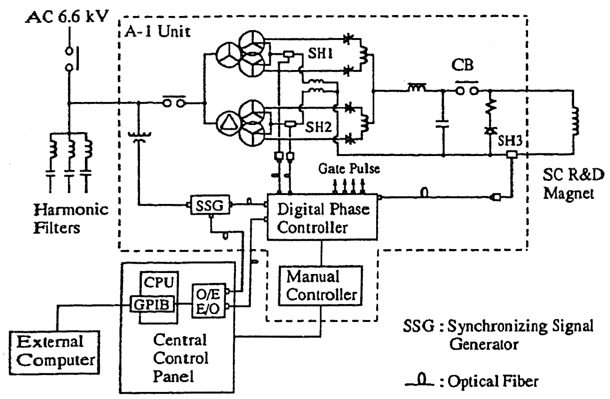

Fig. 2. Control diagram of one unit bank with central panel.

three units of A-1, A-2 and A-3 are used, which can generate the maximum current of 75 kA simultaneously. In order to test scaled-up SC cables in the future, the power supply will be extended to a 100 kA system, by adding an A-4 unit.

The output bus lines are made of aluminum pipes of 180 mm outer diameter with 24 mm thickness. The distance from output terminal of the A-1 unit to the nearest R&D magnet current leads is about 25 m and the voltage drop of this bus line is about 2.5 V. The voltage drop from A-1 unit to the farthest magnet terminal is about 3.5 V. Specifications of a unit bank are listed in Table 1.

Fig. 2 shows a control flow diagram of a unit bank including a central control panel. In order to continuously select the feedback constants and to improve the signal to noise ratio, a digital feedback control method is applied in this power supply. Comparison between the set values and the output values, and the calculating process for the suitable firing angles of the thyristors are carried out on the digital phase controller. To eliminate the electromagnetic noise, the current signals from the shunts and the setting parameters for the output current are converted into digital signals, and transmitted by optical fibers. The available set values for the output current for a unit bank are ; the maximum ramp rate of 999 A/s with a unit of 1 A/s, the maximum current of 25 kA with a unit of 10 A. These set values for the load current, the feedback constants, and operational command can be set, not only from the central control panel, but also from an externally connected computer.

III. CONTROL CHARACTERISTICS OF THE POWER SUPPLY

Fig. 3(a) shows a typical waveform of the measured current in a short-circuit test, operated the maximum ramp rate of 999 A/s for each unit bank with the total flat top of 75 kA. The inductance and resistance in this short-circuit were 6 μH and 66 μΩ, respectively, and the fundamental characteristics of the power supply was investigated in this circuit. As shown in Fig. 3(a), the output current shows a better agreement with the setting values without a response-delay, when using the suitable feedback parameters of proportional and integral (PI) compensation. It was confirmed that the current stability is less than ±0.75% (during 10 minutes) and that the deviation of the measured current from the setting current was less than ±1% at the maximum flat top current.

Fig. 3(b) gives the typical waveform of the measured current with one of the R&D magnets, IV-S & TOKI-PF, which was tested most recently. A little delay of the current rise and a slight over-shoot at the beginning of the holding phase were observed in fast ramp operations. These response delays must be caused by the large dead time of the feedback process and by the insufficiency of the feedback gain. To reduce these problems, we have developed a new algorithm of the digital feedback control system. It will be discussed in the next section.

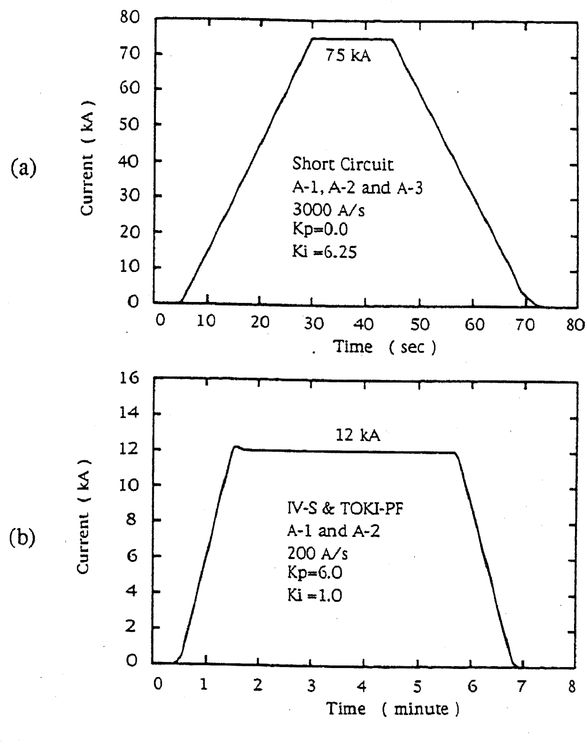

Fig. 3. Typical waveforms of the measured current in a short-circuit test (a) and in the excitation test of one of the R&D magnets (b).

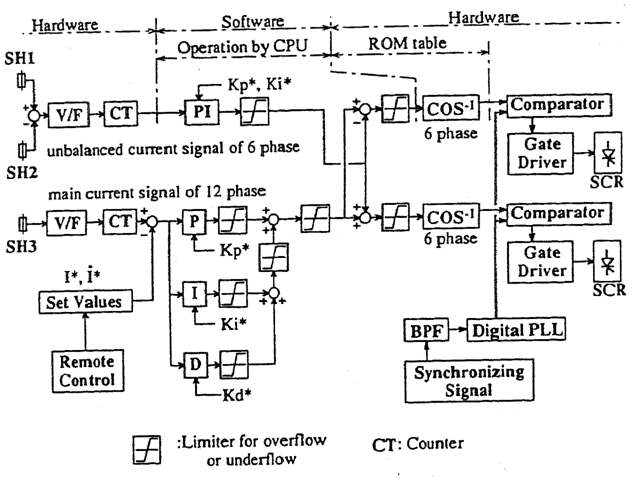

Fig. 4. Algorithm of a new digital feedback control system.

Table 2. Differences of before and after the modification.

Items	Before modification	After modification
Control delay	max. 2.5 Cycle	~1/3 Cycle
Signal converter	A/D converter	V/F converter
Averaging process	Software	Hardware
Gate control	Fixed timer delay	Partial control
Compensation	PI compensation	PID compensation

IV. NEW DIGITAL FEEDBACK CONTROL SYSTEM

The dead time of the feedback loop must be as short as possible, for quick current response. In the original digital feedback system of our power supply system, a maximum dead time of the feedback process was 2.5 cycles of 60 Hz (41.7 ms). The dead time must occur in the averaging process and in the gate control process with a fixed timer-delay for 12-phase thyristors. For shortening the dead time, the defects of the original control method were reviewed, and a new control method was developed.

Fig. 4 shows a new algorithm of the digital feedback control system. On the new feedback control system, the feedback current signals from the shunts are converted to frequency signals (V/F) and are directly averaged by the counters circuits (CT). A shunt of the output circuit, SH3, is used for the main feedback current sensor, to avoid the effect of dc ripple filters, or to eliminate the spike noise from the thyristors. The unbalanced currents from the each 6-phase rectifier detected by the shunts, SH1 and SH2, are converted to the compensation signal of the main feedback loop. The firing pulses of 12-phase thyristors are partially controlled by the phase-locked loop (PLL) circuit and comparator circuits. The PID compensation method is applied in a main feedback process instead of the PI compensation, in order to improve the response in the high frequency region. The differences of before and after the modifications of the feedback control system are listed in Table 2.

V. IMPROVEMENT OF THE CONTROL CHARACTERISTICS

In order to investigate the control characteristics of the modified feedback control system, a small scaled power supply with the output capacity of 20 A and 20 V was prepared. It consists of two double-star rectifier connections to simulate the actual 75 kA power supply system. Experimental set-up used for the frequency response measurement is

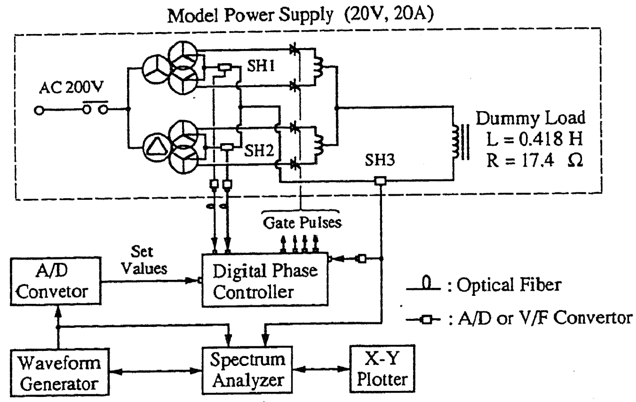

Fig. 5. Experimental arrangement for the digital phase controller.

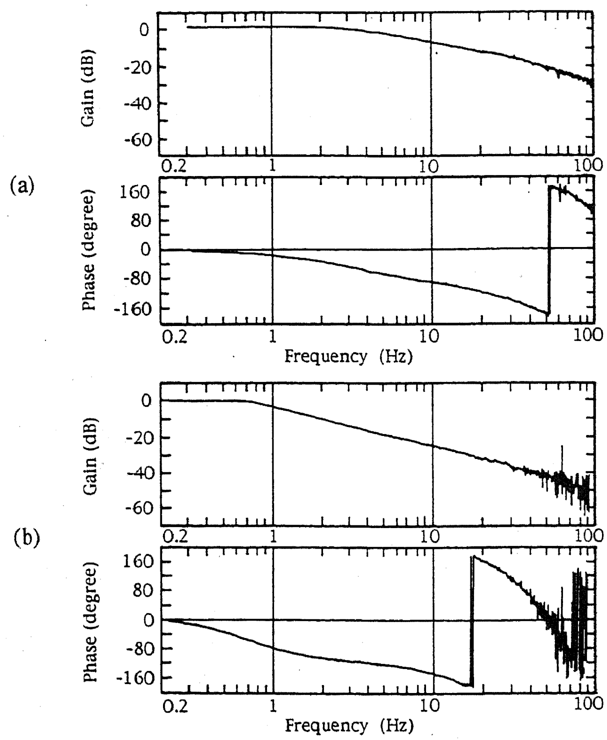

Fig. 6. Measured Bode diagrams of the modified digital phase controller (a), and of the original one (b).

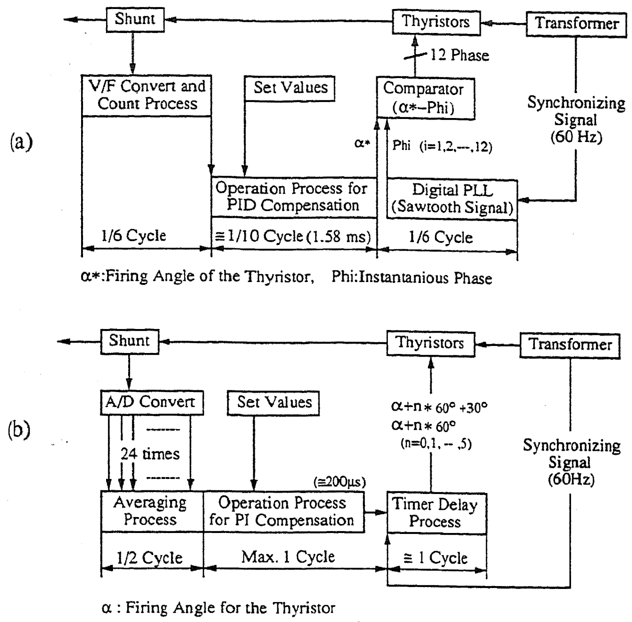

Fig. 7. Comparison of the time-delays of the modified feedback control system (a), and original one (b).

shown in Fig. 5. A Bode diagram of the closed loop can be directly measured in this set-up. Sine-wave signal with variable frequency is fed to a digital phase controller as a set value. The time response of the output current was measured as a function of the frequency. Fig. 6 shows the typical examples of the Bode diagrams measured in the tests of the digital phase controller. In this test, set values of sine-waves and the gains of the feedback loop (Kp, Ki) were kept in the same conditions. The cut-off frequency of 3 dB decrease in the gain property was about 0.9 Hz in the original method, it became 7 Hz in the new method. It is clearly seen that the phase property of the new method has been improved in the high frequency region.

Fig. 7 is a schematic drawings of the time delay process in the digital feedback control system. In the original system as shown in Fig. 7(b), the dominant control delay was caused by the averaging process of the feedback current signals, the watch and wait time to synchronize to the power line of 60 Hz, and fixed firing sequence for 12-phase thyristor. As a result, the total delay was 2.5 cycles of 60 Hz (41.7 ms). The total time of the control delay in the new method is about 6.1 ms, which is reduced to one sixth of that of the original one. As a result, it is confirmed that the maximum available feedback constants, Kp and Ki, can be improved by a factor of two.

The actual inner vertical coil of the LHD, IV-L and IV-U, will be tested in the near future, so that this modification of the control system will be tested for the 75 kA power supply at the same time.

VI. Summary

A dc 75 kA power supply system has been used to test the large scaled SC R&D cables and magnets for the R&D's of LHD. The digital feedback control system was investigated in order to improve the control properties. The results can be summarized as follows: (1) In the original method, maximum dead time of the feedback control process was 41.7 ms. (2) For shotening the control delay, the averaging operation is directly carried out by the V/F convertor and counter circuit. And the firing pulses of the thyristors are partially controlled by the digital PLL and comparator circuits. (3) The dead time of the feedback process is reduced to one sixth, and the feedback gain is improved by a factor of two.

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